

**United** International **University** (UIU)

Dept. of Electrical and Electronic Engineering (EEE)

# Course Code: EEE 442, Title: VLSI Design Lab

**Experiment # 02: Design of a 4-bit Full Adder using Verilog**

Introduction:

1. Follow the steps from lab1 to perform this lab
2. Switch to csh, this will setup your cadence tools environment variables

* csh

1. Create a lab directory and a simulation sub-directory under your work area:

* mkdir lab2
* cd lab2
* mkdir simulation
* cd simulation

1. Write Verilog code for a Half Adder using structural model. Save the file as halfAdder.v

* vi halfAdder.v

1. Write Verilog testbench code for the above Half Adder. Save the file as halfAdder\_tb.v.

* vi halfAdder\_tb.v

1. Simulate the Verilog files and verify the results. Include halfAdder\_tb.v and halfAdder.v
2. Write Verilog code for a 1-bit Full Adder (FA) using the Half Adder (hierarchical structural model). Save the file as fa1bit.v
3. Write Verilog testbench code for the above FA. Save the file as fa1bit\_tb.v
4. Simulate the Verilog files and verify the results. Include fa1bit\_tb.v, fa1bit.v and halfAdder.v Verilog files.
5. Write hierarchical Verilog code for a 4-bit FA using 1-bit FA (use generate block). Save the file as fa4bit.v
6. Write Verilog testbench code for the 4-bit FA. Save the file as fa4bit\_tb.v
7. Simulate the Verilog files and verify the results. Include fa4bit\_tb.v, fa4bit.v, fa1bit.v and halfAdder.v Verilog files.
8. Create a 32-bit FA (behavioral model) and test it.
9. Write Verilog code for 4-bit Subtractor and 4-bit Multiplier.
10. Follow the steps from lab1 to perform this lab